

## REMARKS

Reconsideration of the above-referenced application in view of the following remarks is respectfully requested.

Claims 18-36 are pending in this application. Claims 23-30 were been withdrawn from consideration. No claims are amended herein.

Applicant objects to the withdrawal from consideration of Claims 23-30. The reason given by the Examiner for the constructive election is that an action was received on the merits (presumably before the claims were added). However, Claims 23-30 were added in a Preliminary Amendment mailed 02-27-02. The first action on the merits was mailed by the PTO on 09/16/2002. Therefore, the constructive restriction was improper. Applicant respectfully requests that Claims 23-30 be considered.

Claim 18 stands rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,589,412 to Iranmanesh, et al. Claim 18, as amended, includes the feature of "a substantially planar insulating layer which has portions disposed over said first and second surface portions, said third section extending into said insulating layer, and said insulating layer having first and second recess portions which respectively extend downwardly through said insulating layer toward said first and second surface portions on opposite sides of said third section, each said recess portion being immediately adjacent a respective said side surface of said third section." Iranmanesh does not teach or suggest such a substantially planar insulating layer. Note for example that Iranmanesh's second oxide layer 118 is conformal rather than being substantially planar. Therefore, Applicant respectfully submits that the rejection is improper and that Claim 18 is patentable over Iranmanesh.

Claims 19-22 and 31-36 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Iranmanesh in view of U.S. Patent No. 5,360,757 to Lage. Applicant respectfully traverses the rejection. Claim 18 is nonobvious and patentable over Iranmanesh for the reasons presented above. Lage is cited by the Examiner for its teaching of a composite insulator layer comprising alternating layers of oxide and nitride. Lage does not cure the deficiencies of Iranmanesh. Therefore, Applicant respectfully submits that Claim 18 is patentable over Iranmanesh in view of Lage. Claims 19-22 and Claims 31 and 32 depend from Claim 18 and are therefore patentable over the cited combination of references for at least the reasons presented above. With respect to Claim 20, note that that claim further defines the apparatus of Claim 19 wherein "said first and second portions of conductive material have respective upwardly facing third and fourth surface portions thereon, said third and fourth surface portions being substantially coplanar with a top surface of said insulator layer." Neither Iranmanesh nor Lage teach or suggest such a feature. With respect to Claim 31, Applicant respectfully disagrees with the Examiner's assertion that Iranmanesh at col. 14, lines 6-22 teach side surfaces of a third section having an insulator different from a planar insulating layer. Iranmanesh gives no indication in the cited passage as to what materials he is using or whether they are the same or different from any other material. With respect to Claim 32, Applicant respectfully disagrees with the Examiner's assertion that Iranmanesh teaches at col. 15, lines 23-25 that an insulator is nitride and a substantially planar insulating layer is oxide. Col. 15, lines 23-25 is Iranmanesh's Claim 6, which states that "each intermediate interconnect strip is exposed by a metal bit line opening after every 16 or 32 drain regions." This obviously has nothing to do with the claimed subject matter.

Claim 23 includes the feature wherein "top portions of said first and second terminals are substantially coplanar with said insulating layer covering said top portion of said control terminal." Neither Iranmanesh nor Lage teach or suggest such a feature. Therefore, Applicant submits that Claim 23 is

nonobvious and patentable over those references. Claims 24-26 and Claims 33 and 34 depend from Claim 23 and are therefore patentable over the cited references for at least the reasons presented above. With respect to Claim 33, the Examiner asserts that Iranmanesh at col. 15, lines 23-25 teaches a substantially planar insulating layer coplanar with the insulating layer covering the top portion of the control terminal where in the control terminal and first and second terminals are within an opening in a substantially planar insulating layer. Applicant respectfully disagrees with the assertion. Col. 15, lines 23-25 is Iranmanesh's Claim 6, which states that "each intermediate interconnect strip is exposed by a metal bit line opening after every 16 or 32 drain regions." It is not clear how or whether this passage in Iranmanesh relates to Applicant's claimed invention. With respect to Claim 34, Applicant disagrees with the Examiner's assertion that Iranmanesh at col. 14, lines 6-22 teaches the insulating layer covering the side portions and the top portion of the control terminal is nitride and a substantially planar insulating layer is oxide. Iranmanesh gives no indication in the cited passage as to what materials he is using or whether they are the same or different from any other material.

Claim 27 includes the feature of "local interconnection terminals on opposing sides of said gate stack and abutting said insulating material on said side portions of said gate electrode, said local interconnection terminals extending above said plane of semiconductor material such that top portions of said local interconnection terminals are substantially coplanar with said insulating material covering said top portion of said gate electrode." Neither Iranmanesh nor Lage teach or suggest such a feature. Therefore, Applicant submits that Claim 27 is nonobvious and patentable over those references. Claims 28-30 and new Claims 35 and 36 depend from Claim 27 and are therefore patentable over the cited references for at least the reasons presented above. With respect to Claim 35, Applicant disagrees with the Examiner's assertion that Iranmanesh at col. 14, lines 6-22 teaches a substantially planar insulating layer coplanar with an insulating material covering the side and top portions of the gate stack

wherein the gate stack and local interconnection terminals are within an opening in the substantially planar insulating layer. The cited passage of Iranmanesh does not describe an opening in a planar insulating layer. With respect to Claim 36, Applicant disagrees with the Examiner's assertion that Iranmanesh at col. 15, lines 23-25 teaches an insulating layer material covering the side and top portions of the gate stack is nitride and the substantially planar insulating layer is oxide. Col. 15, lines 23-25 is Iranmanesh's Claim 6, which states that "each intermediate interconnect strip is exposed by a metal bit line opening after every 16 or 32 drain regions." This obviously has nothing to do with the claimed subject matter.

Applicant respectfully requests reconsideration and withdrawal of the rejections and allowance of Claims 18-36. If the Examiner has any questions or other correspondence regarding this application, Applicant requests that the Examiner contact Applicant's attorney at the below listed telephone number and address.

Texas Instruments Incorporated  
P.O. Box 655474, M/S 3999  
Dallas, TX 75265  
Phone: 972 917-5653  
Fax: 972 917-4418

Respectfully submitted,



Michael K. Skrehot  
Reg. No. 36,682